Name: _____

CIS 351 Sample ADD3 Problem

06 January 2022

ADD3: Carry Lookahead Adder

(a) Sketch the lookahead logic for the carry into column 4. (Columns are indexed beginning with 0.)

(b) Suppose one were to make a mistake and accidentally use an `AND` gate in place of the rightmost `OR` gate for the carry lookahead logic. Describe the inputs A and B that would produce a value of 1 on the carry out.

Name: _____

ADD4: Carry Select Adder

(a) Sketch the top-level of a 16-bit carry-select adder.

(b) Assume that the carry-select pattern is applied at only the top-level, and that the component 8-bit adders are standard ripple-carry adders. Fill in the blanks: The propagation delay of this carry select adder is _____ (more than, exactly, less than) _____ (give a fraction) that of a 16-bit ripple carry adder.

(c) Explain your choice of "more than", "exactly", or "less than" for the previous problem.