Name: _____

Practice Test 2

Updated: February 17, 2019

Test 2 is Friday, 1 March.

1. How does the multi-cycle CPU attempt to improve performance?
2. Suppose the longest instruction in a multi-cycle CPU requires k cycles. Suppose also that the corresponding single-cycle CPU has a clock period of p. Will the multi-cycle CPU's clock period be faster, slower, or similar to $\frac{p}{k}$? Why?
3. What are the key principles of RISC and CISC?
4. How do multi-cycle CPUs tend to exemplify the CISC philosophy?
5. Be able to list the micro-instructions for those MIPS instructions you implemented in the microcode assignment.
6. Consider a `swap` instruction that swaps the values in two registers.
   (a) It is not possible to implement this instruction without additional data paths and/or muxes. Why not?
   (b) Add the necessary additional data paths / muxes to the figure below.
   (c) List the micro-instructions that will implement `swap`.
   (d) List the values of the control wires that will implement the microinstructions you listed in part 6c
7. With the multi-cycle CPU, we no longer need a register file with two read ports. Describe what changes you would need to make to the multi-cycle CPU to support a single-ported register file.
8. What are control hazards?
9. How do branch predictors address control hazards?
10. Explain the difference between static and dynamic branch prediction.
11. What is a tournament predictor? Why are tournament predictors used?
12. Explain the difference between global and local branch prediction.
13. Describe the operation of a two-level adaptive branch predictor.
14. Is the two-level adaptive branch predictor primarily a local predictor, or primarily a global predictor. Explain your reasoning?