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CS451 Branch Prediction Homework

1. You are asked to design a pipelined CPU that has no branch penalties at all: It has no branch delay slots, and does not rely on branch prediction.

   (a) What must you do to implement such a CPU?

   (b) What are the major limitations of this design?

2. Suppose that a machine with a 5-stage pipeline uses branch prediction (i.e., no branch delay slots). 15% of the instructions for a given test program are branches, of which 80% are correctly predicted. The other 20% of the branches suffer a 4-cycle mis-prediction penalty. (In other words, when the branch predictor predicts incorrectly, there are four instructions in the pipeline that must be discarded.) Assuming there are no other stalls, develop a formula for the number of cycles it will take to complete n lines of this program.

3. Now suppose you are given the option of replacing this processor's branch prediction scheme with a 1-cycle branch delay system (i.e., there is one branch delay slot after every branch). What percentage of the branch delay slots must be filled in order for the CPU with the branch-delay system to have better performance than the CPU described in question 2?

4. Consider two pipelined CPUs that uses branch prediction.

   - CPU A has a 200ps cycle time and a 5-cycle branch penalty.
   - CPU B has a 175ps cycle time and a 8-cycle branch penalty.

   (a) For which instruction mixes is CPU B faster when the branch predictor has an 85% accuracy? (You only need specify the percent of instructions that are branches.)

   (b) Does increasing the accuracy of the branch predictor increase or decrease the percentage of branch instructions that allow CPU B to be faster? Why?

5. You have a pipelined CPU that uses branch prediction. The penalty for a mis-predict is 4. Your employer proposes doubling the pipeline depth. Doing so will reduce the clock period by 25%; but will double the branch penalty. Your task is to figure out if this design change will improve performance. The performance improvement depends on two factors: the accuracy of the branch predictor, and the percentage of instructions that are branches.

   Let b be the percentage of instructions that are branches. Let m be the branch predictor's *mis-predict* rate.

   (a) Develop (and simplify) a formula that describes the performance of the original CPU in terms of b and m.

   (b) Develop (and simplify) a formula that describes the performance of the new CPU in terms of b and m.

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(c) Develop (and simplify) a formula that determines how accurate the branch predictor must be given the percentage of instructions that are branches. (In other words, generate a formula that solves for m in terms of b.)

(d) At what accuracy does the percentage of branch instructions become irrelevant?

(e) At what what point does the accuracy of the branch predictor become irrelevant?

6. Problem 6.36 from Patterson and Hennessy: Compute the predictions for each predictor and branch pattern. Specifically, indicate how each branch will be predicted, then give the hit rate. Use the 2-bit predictor shown in Figure 1.

Predictor	TTT	NNN	TNTNTN	TTTNT	TTNTTNT
Always Taken					
Always not-taken					
1 bit predictor (init. to predict taken)					
2 bit predictor (init. to *weakly* taken)					
2 bit predictor (init. to *strongly* taken)					
2 bit predictor (init. to *weakly* not-taken)					
2 bit predictor (init. to *strongly* not-taken)					

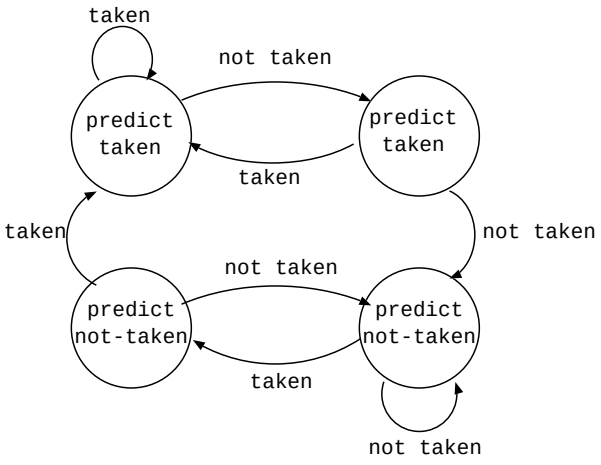

Figure 1: 2-bit branch predictor