Learning Objectives

CIS 351 — Fall 2026

Number Representation

- NR1[i] Binary
  a. Convert from positive decimal integers to binary
  b. Convert from binary to positive decimal integers
  c. Determine the range of non-negative integers that can be represented using n binary bits
  d. Determine the number of bits necessary to store positive integers up to x
  e. Continue a sequence of binary values (up or down) without converting to decimal (or any other base)
- NR2 Two's Complement
  a. Convert from any decimal integer to two's complement (using the correct number of leading 1s for the given number of bits)
  b. Convert from two's complement to any decimal integer
  c. Determine the number of bits necessary to store integers between x and y in two's complement form
  d. Continue a sequence of two's complement values (up or down) without converting to decimal (or any other base)
- NR3 Hexadecimal
  a. Convert directly from binary to hexadecimal (i.e., do not convert to decimal or any other representation as an intermediate step)
  b. Convert directly from hexadecimal to binary (i.e., do not convert to decimal or any other representation as an intermediate step)
  c. Continue a sequence of hexadecimal values (up or down) without converting to decimal (or any other base)
- NR4 Other Number Bases
  a. Convert from base 10 to any base (positive integers only)
  b. Convert from any base to base 10 (positive integers only)

Combinatorial Logic

- CL1[i] Create a truth table that describes a problem (e.g., a truth table that represents the desired outputs of a 4-bit "isPrime" circuit)
- CL2 Read a circuit description
  a. Complete a truth table that describes the output of a circuit described by a Boolean expression
  b. Complete a truth table that describes the output of a circuit described by a circuit diagram.
- CL3 Write a Boolean expression
  a. Write a Boolean expression in sum-of-products form that describes a given truth table
  b. Write a Boolean expression that describes the behavior of a given combinatorial circuit
- CL4 **(Core)** Draw a circuit diagram
  a. Draw a circuit that implements a given truth table
  b. Draw a circuit that represents the implementation of a given Boolean expression
- CL5 **(Core)** Determine the propagation delay of a combinatorial circuit
- CL6 **(Core)** Design a combinatorial circuit that uses basic gates, multiplexors, demultiplexors, adders, and subtractors.

Addition

- ADD1[i] Directly compute the sum of two numbers written in binary
- ADD2[i] Demonstrate knowledge of the operation of a ripple-carry adder
- ADD3 Demonstrate knowledge of the operation of a non-linear adder
  a. Carry-lookahead
  b. Carry-select
- ADD4 Recognize when the addition of x and y will produce overflow
- ADD5[p] Demonstrate how to detect overflow when adding two numbers

Functional Completeness

- FC1 Write the outline of a proof of logical/functional completeness. This outline should clearly indicate that the student knows which "direction" the proof should go (i.e, that you use NAND to build AND, OR, NOT as opposed to using AND, OR, NOT to build NAND).
- FC2^{h} Write a complete proof of logical/functional completeness.

Boolean Algebra

- BA1 **(Core)** Simplify a Boolean expression by applying DeMorgan's laws as well as the commutative, associative, and distributive properties to a Boolean expression (including factoring) then canceling terms when appropriate

Sequential Logic

- SL1 Latches
  a. Explain how a feedback loop can be used to store data
  b. Complete the characteristic table of a sequential circuit that uses feedback but no clock (i.e.,the NOR latch)
  c. Incorporate a latch into a more complex sequential circuit (e.g., incorporate a NOR-latch into a D-Latch)
  d. Add a clock to a latch
- SL2 Flip-Flops
  a. Explain the operation of a master-slave (or similar) flip-flop (e.g., what gives the flip-flop its "instant" trigger point).
  b. Use a timing diagram to demonstrate the internal behavior of a master-slave flip-flop.
  c. Describe the behavior of a master-slave flip-flop (e.g., by completing a timing diagram)
- SL3^{lf} *(not used W22)* Demonstrate what goes wrong with traditionally-designed combinatorial circuits if clocks aren't present.
- SL4 **(Core)** Trace the behavior of a a sequential circuit that contains a flip-flop and a clock
  a. Write the characteristic table of a sequential circuit that contains a flip-flop and a clock
  b. Draw the timing diagram for a sequential circuit with given input and initial state

- SL5[i] Construct a circuit diagram given a characteristic table
- SL6 **(Core)** Design a sequential circuit that uses flip-flops, basic gates, multiplexors, demultiplexors, adders, and subtractors.

Assembly Language

- AL1[i] Translate a single, complex arithmetic expression (e.g. $x = (y + z) - (w + t)$) into a sequence of assembly statements.
- AL2 **(Core)** Translate an `if-else` statement into a sequence of assembly statements
- AL3 **(Core)** Translate a `for` loop into a sequence of assembly statements
- AL4 **(Core)** Write "intermediate" assembly by hand
  a. Write an assembly function that iterates over an array or string and examines/processes each item (e.g., sum the values in an array, or count the vowels in a string)
  b. By hand, write an assembly function that iterates over an array or string and manipulates some of the items (e.g., iterate over an array of integers and set each negative value to 0)
- AL5 Read assembly code
  a. Describe the behavior of an assembly language function containing branches at a high level
  b. Describe the behavior of an assembly language function containing loops at a a high level
  c. Describe the behavior of an assembly language function that uses the offset parameter for memory operations
- AL6[h] Write, test, and debug assembly code.
  a. Write, test, and debug an assembly function that uses if-else, loops, and memory accesses
  b. Write, test, and debug assembly code that uses the offset parameter for memory accesses
  c. Write assembly code containing multiple functions that correctly uses MIPS conventions for calling functions (a0-a4 for parameters and v0 for return values)
- AL7[l] Write assembly code containing multiple functions (including non-leaf functions) that use MIPS conventions for saving and preserving registers when necessary
- AL8[lf] *(not used W22)* Explain how the use of the stack enables recursion

Single Cycle CPU Design/Implementation

- SS1[h] Machine Language
  a. Assemble machine instructions "by hand"
  b. Disassemble machine instructions "by hand"
- SS2[p] Build a single cycle CPU using a digital logic simulator such as JLS
- SS3 **(Core)** Describe the operation of the single-cycle CPU
  a. Identify the value on any given wire given a specific instruction
  b. Describe the purpose of the value on a specific wire (i.e., how it is used).
  c. Describe the consequences of a particular wire being "broken".
  d. Identify the width of a given wire
- SS4 Make a small change to the design of a single-cycle CPU (e.g., add or modify an instruction)
- SS5 Single-Cycle Design and Patterson and Hennessey's Four Design Principles
  a. Explain the reasoning behind the design decisions in the example Single Cycle CPU (motivation for each instruction type, why each field has the size it does, fixed vs. variable width, absolute vs. relative addresses for branches and jumps, use of function code etc.) In most cases, explanations should reference Patterson and Hennessey's four design principles.
  b. Given a particular CPU design choice (e.g., I-type instructions) list and explain alternate choices as well as the benefits and costs of each.
  c. Explain the benefits of the MIPS offset addressing mode. Describe alternatives to this addressing mode and the pros and cons of each alternative

Cache and Memory

- M1[i] Compare and contrast the construction / operation of DRAM vs. SRAM. Explain why SRAM is faster but more expensive.
- M2 **(Core)** Cache mechanics
  a. Given a cache configuration, determine the number of index, offset, and tag bits
  b. Compute the total size of the cache
  c. Sketch the cache's configuraiton
- M3 **(Core)** Trace the hits and misses in a cache

- M4 **(Core)** Cache parameters
    a. Explain the effects of modifying basic cache parameters (e.g., increasing and/or decreasing a cache's block size)
    b. Identify whether a program would benefit from a large or small block size
    c. Identify whether a program would benefit from a larger associativity

Pipeline

- P1 **(Core)** Basic Pipeline concepts
- P2 Data and Control Hazards

Key

i	Implicit:	This objective will not be evaluated explicitly. Knowledge of this objective is necessary to successfuly master other objectives.
h	Homework:	This objective is satisifed by completing a homework assignment.
l	Lab:	This objective is satisfied by completing a lab.
p	Project:	This objective is satisfied by completing a project.
f	Future:	This objective will not be used this semester.

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