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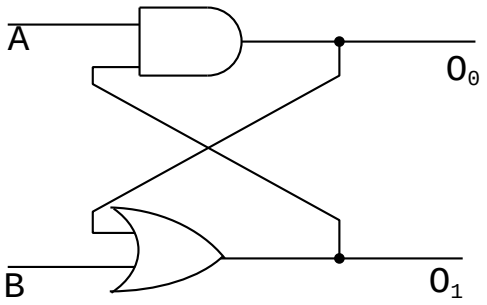
# CIS 351 Sequential Circuit Homework

1. Complete the characteristic table for the circuit shown below: Note, there is no clock pulse here. Your answers should show the states $Q$ and $\bar{Q}$ after they have reached a steady state given $A$, $B$, and current values of $O_0$ and $O_1$. If the given inputs will produce a non-deterministic output (i.e., the output depends on which gate changes first), write "random" in the row.

| A | B | $O_{0_{now}}$ | $O_{1_{now}}$ | $O_{0_{next}}$ | $O_{1_{next}}$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | | |
| 0 | 0 | 0 | 1 | | |
| 0 | 0 | 1 | 0 | | |
| 0 | 0 | 1 | 1 | | |
| 0 | 1 | 0 | 0 | | |
| 0 | 1 | 0 | 1 | | |
| 0 | 1 | 1 | 0 | | |
| 0 | 1 | 1 | 1 | | |
| 1 | 0 | 0 | 0 | | |
| 1 | 0 | 0 | 1 | | |
| 1 | 0 | 1 | 0 | | |
| 1 | 0 | 1 | 1 | | |
| 1 | 1 | 0 | 0 | | |
| 1 | 1 | 0 | 1 | | |
| 1 | 1 | 1 | 0 | | |
| 1 | 1 | 1 | 1 | | |




2. Choose a row from problem 1 labeled "random", and explain why the output is random.

3. The above circuit can be used as a latch (provided you avoid the inputs that lead to random state). What input combinations can be used for "set", "reset", and "hold"? (Hint #1: One or both of the inputs may be "active low". Hint #2: Don't assume that $O_0$ and $0_1$ should necessarily hold oppostite values — that's why they aren't labeled $O$ and $\bar{O}$.)

4. One of the four input combinations should be avoided. List the input combination that should be avoided, then explain specifically what goes wrong if that combination is used.

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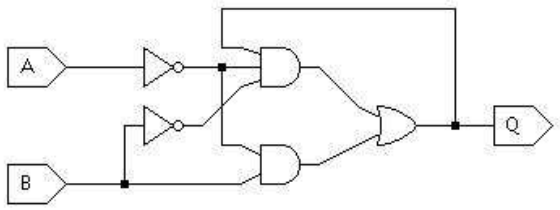
5. Consider the circuit shown below and to the rigth:

   (a) Complete the characteristic table for the circuit shown below:

| $A_n$ | $B_n$ | $Q_n$ | $Q_{n+1}$ |
|---|---|---|---|
| 0 | 0 | 0 | |
| 0 | 0 | 1 | |
| 0 | 1 | 0 | |
| 0 | 1 | 1 | |
| 1 | 0 | 0 | |
| 1 | 0 | 1 | |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | |




   (b) What fundamental sequential circuit has the same characteristic table?

   (c) Use Boolean Algebra to show how the circuit you identified in problem 5b is equivalent to one in the diagram above.

6. A JK flip-flop has the following characteristic table. In the space on the right, show how you can use a D flip-flop and some combinatorial logic to construct a JK flip-flop. (Note: The idea here is to use a D flip-flop as the core of your circuit. It is also possible to build a JK flip-flop directly from gates and/or transistors; but, that's not what this problem is about.)

| J | K | $Q_n$ | $Q_{n+1}$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

7. Complete the characteristic table for the circuit shown below: (See problem 6 for the definition of a JK flip-flop.)

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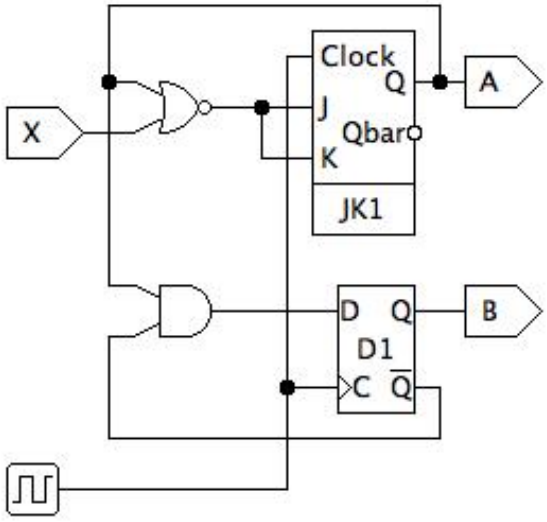
| $X$ | $A_n$ | $B_n$ | $A_{n+1}$ | $B_{n+1}$ |
|---|---|---|---|---|
| 0 | 0 | 0 | | |
| 0 | 0 | 1 | | |
| 0 | 1 | 0 | | |
| 0 | 1 | 1 | | |
| 1 | 0 | 0 | | |
| 1 | 0 | 1 | | |
| 1 | 1 | 0 | | |
| 1 | 1 | 1 | | |



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8. Consider the sequential circuit shown below:

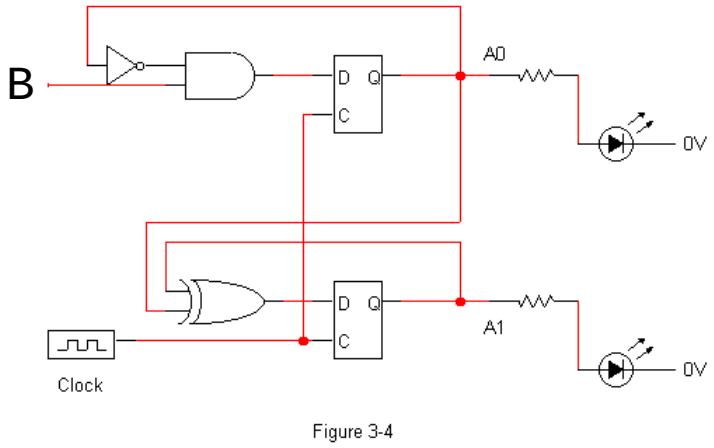
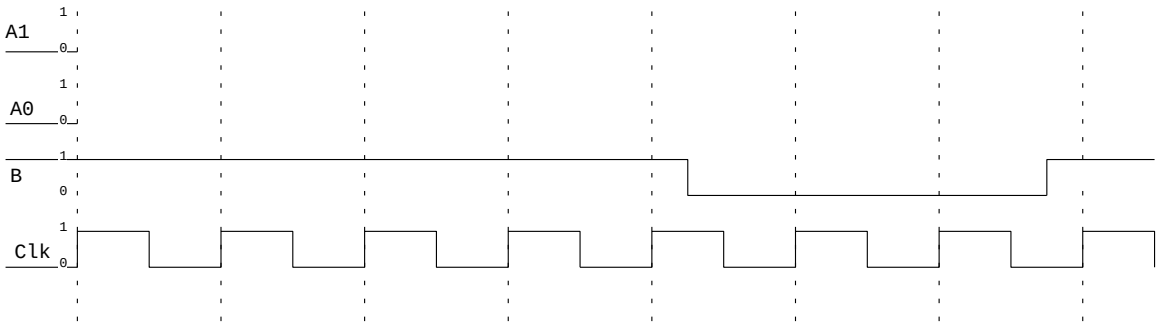



Figure 3-4

(a) First, complete the characteristic table. This circuit is clocked; and all flip flops are *positive-edge triggered*. Your answers should show the states of $A_0$ and $A_1$ after the next clock pulse.

| Current state | | | State after next clock pulse | |
|---|---|---|---|---|
| $B$ | $A_0$ | $A_1$ | $A_0$ | $A_1$ |
| 0 | 0 | 0 | | |
| 0 | 0 | 1 | | |
| 0 | 1 | 0 | | |
| 0 | 1 | 1 | | |
| 1 | 0 | 0 | | |
| 1 | 0 | 1 | | |
| 1 | 1 | 0 | | |
| 1 | 1 | 1 | | |

(b) Now complete the following timing diagram ($\Delta t$ not required). Again remember that the flip-flops are positive-edge triggered. This means that $A_0$ *and* $A_1$ *will change* **only** *when the clock rises from 0 to 1!*



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9. Design a circuit that has the following characteristic table. (Hint: Connect two D-latches in a manner similar to that shown in problem 8.)

| Current state | | | State after next clock pulse | |
|---|---|---|---|---|
| $B$ | $A_0$ | $A_1$ | $A_0$ | $A_1$ |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 |

10. Design a sequential circuit that can add arbitrarily large numbers. This circuit will have three input pins: $A_n$, $B_n$, and "reset". "Reset" indicates that a new addition is beginning. $A_n$ and $B_n$ take one "column" of input on each clock pulse. The circuit has one bit of output, which is the sum of the column currently being calculated.

11. Design a sequential circuit that will examine a sequence of characters and determine whether all five vowels are present in the string. The circuit will have one 8-bit input that will contain the ASCII representation of a character. On each clock tick, the input will contain the next character in the sequence. The circuit also has a 1-bit output that is initially `false` and becomes `true` once all five vowels have been observed. You may treat sub-circuits "`is a`", "`is e`", "`is i`", "`is o`", and "`is u`" as "black boxes".

12. Design a sequential circuit to run a countdown timer. This circuit should contain two registers: One for the minutes and one for the seconds. Decrement the seconds every time the clock ticks. Stop decrementing when the timer reaches 0. This circuit should have three outputs: `minutes`, `seconds`, and a one-bit `alarm` output that will be set to 1 when the timer reaches 0.

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13. For more practice (not due for credit): Consider the "old" automatic doors — the ones with sensors on the ground that tell the door when to open an close.

    (a) Design a finite state machine to describe the operation of a one-way door. Each sensor provides a binary input (the presence or absence of a person).

    (b) Design a circuit to implement this state machine.

    These doors have sensors on both sides because (1) you don't want the door to hit anybody standing outside, and (2) you don't want the door to close in somebody's face.

    To be clear: You are designing the circuit for one door. Typically, these doors come in pairs (an "in" and and "out"); each door will have its own circuit.


14. For more practice (not due for credit): Consider a simple DVD/BluRay player. The playback mode is controlled by three buttons: Play/Pause, Fast Forward, and Rewind.

    There are three "fast forward" speeds. To get to the faster speeds, press the fast forward button multiple times. Likewise for reverse.

    - Pressing "Play" while fast forwarding or rewinding returns the player to the "normal" forward speed.
    - Pressing "Fast Forward" while in the highest speed returns the player to normal forward speed. Likewise for reverse.
    - Pressing "Rewind" while in fast forward mode reduces the speed one level. Likewise for Fast Forward.

    (a) Design a finite state machine to describe the operation of this player.

    (b) Design a circuit to implement this state machine.