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Practice Test 1

Draft 1 October 2018

Test 1 is Tuesday, 9 October. Problems 24, 33, and 34 are due for credit Friday, 5 October.

Also, pay special attention to problems 21, 36, 37, and 38.

For the real test, you will need to show your work in order to receive any partial credit.

1. Convert 100_{10} into an unsigned binary number. _____
2. Convert 100_{10} into a hexadecimal number. _____
3. Convert 100_{10} into a base 3 number. _____
4. What is the standard range of numbers that can be represented by an 8 bit *unsigned* binary number? _____
5. What is the standard range of numbers that can be represented by a 10 bit *signed* binary number? _____
6. How many bits are needed to represent -200 as two's complement binary number? _____
7. Convert -200_{10} into a 12 bit two's complement binary number. _____
8. Convert the unsigned binary number 11001110 into decimal. _____
9. Convert the unsigned binary number 1100000011011110 into hexadecimal. _____
10. Convert 1234_5 to decimal. _____
11. Convert `0xBAD4F00D` to binary. _____
12. Convert the 10 bit two's complement binary number 1101100100 to decimal. _____
13. Write the six binary numbers that follow 1101.

    1) _____
    2) _____
    3) _____
    4) _____
    5) _____
    6) _____

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14. Write the six two's complement binary numbers that precede 0010.

    1) _____
    2) _____
    3) _____
    4) _____
    5) _____
    6) _____

15. Write the eight hexadecimal numbers that follow `0x1C99`.

    1) _____
    2) _____
    3) _____
    4) _____
    5) _____
    6) _____
    7) _____
    8) _____

16. Add $10110 + 01101$ in binary.

17. Add $133_4 + 321_4$ in base 4.

18. Complete the following truth tables:

A	B	C	$(A \oplus B) \oplus C$
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

A	B	C	$\bar{A}\bar{B} + B(A + \bar{C}) + \overline{BC}$
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

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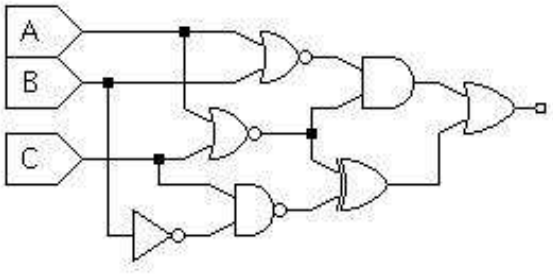
19. Draw the logic diagrams for the following boolean expressions:

    (a) $\bar{A}\bar{B} + B(A + \bar{C}) + \overline{BC}$

    (b) $\bar{X} + X(X + \bar{Y})(Y + \bar{Z})$

    (c) $(A + B)\overline{(\bar{A} + \bar{B})}$

20. Write a Boolean expression that describes this circuit:



21. Given the gate timings below, what is the total propogation delay of the circuit in problem 20? (In other words, how long must you wait to be sure the output of your circuit has the correct, final value?)

AND	5
OR	5
NOT	3
NAND	3
NOR	5
XOR	5

22. Given the timings in problem 21, highlight the critical path in the circuit from problem 20.

23. Show that {AND, NOT} is logically complete.

24. Show that a 2-to-1 mux is logically complete for 2-input gates. (Hint: Tie some of the mux's inputs to `true` or `false`.)

25. Design a circuit that returns true if the input represents the integer 10, and false otherwise.

26. Use Boolean algebra, including DeMorgan's laws to show the equivalence of each pair of expressions. Show all your work. You may not use truth tables.

    (a) $\bar{X} + X(X + \bar{Y})(Y + \bar{Z}) \iff \bar{X} + Y + \bar{Z}$

    (b) $(A + B)\overline{(\bar{A} + \bar{B})} \iff AB$

    (c) $(B + \bar{C} + \bar{A}B)(BC + A\bar{B} + AC) \iff BC + A\bar{B}\bar{C}$

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27. Show how to build a full adder using two half-adders. (A half adder takes two inputs a and b, and has two outputs *out* and *carry*. Unlike a full adder, it does not have a *carryin* input.)

28. Explain, at a high level, how a carry lookahead adder works, why it is faster than a ripple carry adder, and what tradeoff is made when using a carry lookahead adder.

29. Draw a 2x4 decoder using only 2-input AND, OR, NOT, and XOR gates.

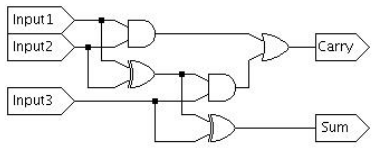
30. Draw a 4-to-1 multiplexer using only 2-input AND, OR, NOT, and XOR gates. If you wish, you may also use a decoder.

31. Sketch a 4-bit ripple carry adder.

32. Design a circuit that takes two n-bit inputs and returns `true` if the two inputs are identical and `false` otherwise.

33. Design a circuit that increments the hours and minutes on a 24-hour clock. This circuit has a 5-bit input representing hours and a 6 bit input representing minutes. It also has a five-bit output representing the updated hour and a 6-bit output representing the updated minute. The outputs should represent one minute after the inputs. For example, if the inputs are 6 and 10, then the outputs should be 6 and 11. If the inputs are 7 and 59, then the outputs should be 8 and 0. If the inputs are 23 and 59, then the outputs should be 0 and 0.

34. Compute the worst-case gate delay for both ripple-carry adders shown below. Both adders use the same full adder (shown at right). Show your work (i.e., explain how your arrived at your answer).



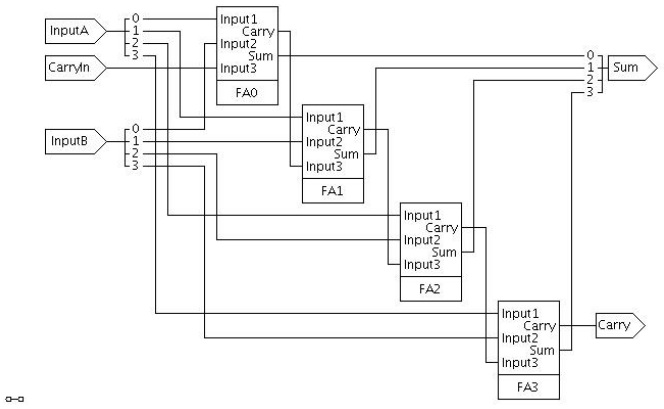


Figure 1: "Fast" Ripple-carry adder

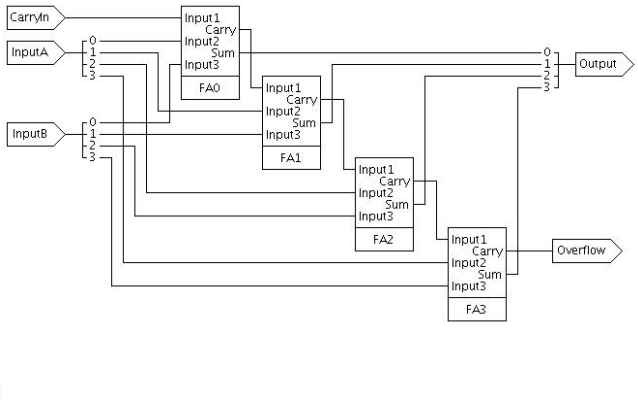


Figure 2: "Slow" Ripple-carry adder

35. For each circuit in problem 34, find an example input that requires the maximum amount of time.

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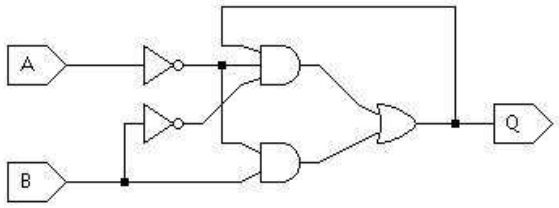
36. Complete the characteristic table for the circuit shown below:

A_n	B_n	Q_n	Q_{n+1}
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

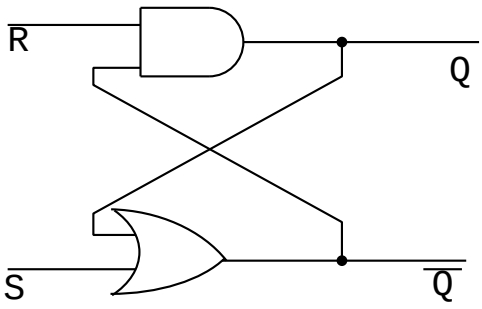


What fundamental circuit has the same characteristic table?

37. Use Boolean Algebra to show how the circuit in problem 36 is equivalent to one of the fundamental circuits used to build CPUs.

38. Complete the characteristic table for the circuit shown below: Note, there is no clock pulse here. Your answers should show the states Q and $\bar{Q}$ after they have reached a steady state given R, S, and current values of Q and $\bar{Q}$. If the given inputs will produce a non-deterministic output (i.e., the output depends on which gate changes first), write "random" in the row.

R	S	Q_{now}	$\bar{Q}_{now}$	Q_{next}	$\bar{Q}_{next}$
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		
0	1	0	1		
0	1	1	0		
0	1	1	1		
1	0	0	0		
1	0	0	1		
1	0	1	0		
1	0	1	1		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		



39. Choose a row labeled "random", and explain why the output is random.

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40. Show how to build a SR latch (clocked or unclocked).

41. Show how to build a D latch (clocked or unclocked).

42. Show how to build a D flip-flop from two D latches.

43. Show how to add an `e`nable input to a D latch or flip-flop.

44. Review the Sequential Circuits homework.

45. Design a sequential circuit to run a countdown timer. This circuit should contain two registers: One for the minutes and one for the seconds. Decrement the seconds every time the clock ticks. Stop decrementing when the timer reaches 0. This circuit should have three outputs: `minutes`, `seconds`, and a one-bit `alarm` output that will be set to 1 when the timer reaches 0.